

ONE TIME EXIT SCHEME

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10CS74

Seventh Semester B.E. Degree Examination, April 2018

Advanced Computer Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Define computer Architecture and explain the seven dimensions of ISA. (10 Marks)
b. Find the number of dies per 300mm wafer of circular shape that is used to cut a die that is 1.5cm on side and compare the result with value 1.25. (04 Marks)
c. Explain the quantitative principles of computer design. (06 Marks)
- 2 a. Explain Classic 5 stage pipeline in RISC processors. (10 Marks)
b. List and explain the major hazards in pipeline. Illustrate hazards with examples. (10 Marks)
- 3 a. List and explain the different types of dependencies with example. (08 Marks)
b. With an appropriate example explain Rescheduling and loop unrolling. (08 Marks)
c. With the neat sketch explain dynamic branch prediction. (04 Marks)
- 4 a. Explain Tomasulo algorithm for extended support speculation. (10 Marks)
b. Explain the basic VLIW approach. List the drawbacks. (10 Marks)

PART – B

- 5 a. With neat sketch explain the basic structure of centralized shared memory architectures and distributed memory multiprocessors. List the advantages and disadvantages. (10 Marks)
b. Explain the basic schemes for enforcing coherence. (10 Marks)
- 6 a. With neat sketch explain the hypothetical memory hierarchy. (05 Marks)
b. Explain the three block replacement strategies when cache miss occurs. (06 Marks)
c. Explain the six basic cache optimization techniques. (09 Marks)
- 7 a. Briefly explain the eleven advanced cache optimization techniques. (11 Marks)
b. Write a note on protection of virtual memory and protection with virtual machines. (09 Marks)
- 8 a. Explain in detail the hardware support for preserving exception behavior during speculation. (10 Marks)
b. Write a note on :
 - i) IA – 64 register models
 - ii) The Itanium 2 processor. (10 Marks)

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